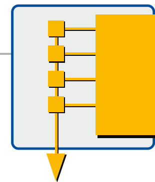
Simple Test of Complex Things

Production-Oriented Assembly and System Test



Do you still **waste** valuable **time** when taking your prototypes into operation?

Simple troubleshooting via detailed and graphical fault analysis

JTAG

Do you still **awkwardly** solder your flash components for **programming**?

In-system programming of ICs from all vendors through one tool

BScan!

Do you still ask yourself how to **measure** the **levels** on your **BGA pins**?

Access to all digital component pins via four-wire-bus

by GÖPEL electronic

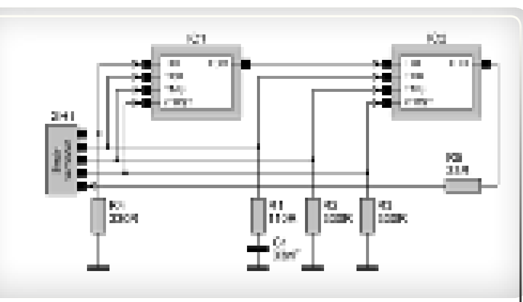
JTAG / Boundary Scanis your solution – all you need is a fistful of design rules!

GÖPEL electronic

Get the total Coverage!

Five Design Rules for JTAG / Boundary Scan

IEEE 1149.1 standard conformity



Shift chain layout

Excerpt from a BSDL file

1. IC Selection

As many Boundary Scan enabled ICs (integrated circuits) as possible should be utilised to achieve the highest test coverage. On the one hand, a higher test coverage is obtained because a larger number of pins testable by Boundary Scan can be contacted. On the other hand, even more precise diagnostic are possible if several of such pins exist on a net.

How do you now if your component can be tested via Boundary Scan? Have a look in the component's data sheet and check for information about IEEE 1149.1 standard conformity.

2. Shift Chain Layout

Connect the Boundary Scan ICs to one or several shift chains. Pay attention to correct layout and test bus signal schedule.

3. General Conditions

Compliance conditions determine the pin connections to enable Boundary Scan tests. The respective section starts with the attribute "COMPLIANCE_PATTERNS", being an optional part of the BSDL file.

4. Programming of Large Data Sets

There are often opportunities for speed optimisation, e.g. by external access to the write signal during flash programming. Enable this access, for instance by an additional signal in your JTAG connector.

5. Access to Structures not Testable with Boundary Scan

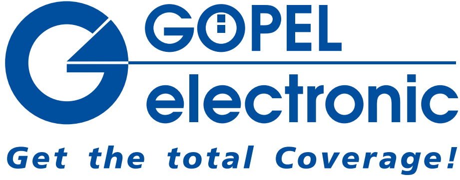
Many ICs not testable by Boundary Scan can mostly be checked by other test methods, such as a NAND-tree test. These tests can be switched on and off via a pin. Connect this pin with a Boundary Scan IC to include the non-Boundary Scan ICs into your test.

Glossary

BGA – *Ball Grid Array*
Housing type with ball-shaped pins at the chip's bottom side

BSDL – *Boundary Scan Description Language*
Language to describe Boundary Scan abalities

IEEE 1149.1 – *Boundary Scan Standard*
Describes the static digital connection test (a.o. the BSDL file structure)



ISO 9001 certified

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