Applikation

JTAG/Boundary Scan

BSDL Verification • Design Validation • Hardware Debugging • Component Programming • Structural Test • Functional Test • Emulation Test • Mixed Signal Test • Optoelectric Test

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Get the total Coverage!

Versatile JTAG/Boundary Scan Application

The V-Model Leads the Way

Each product life cycle is defined by the following stages:

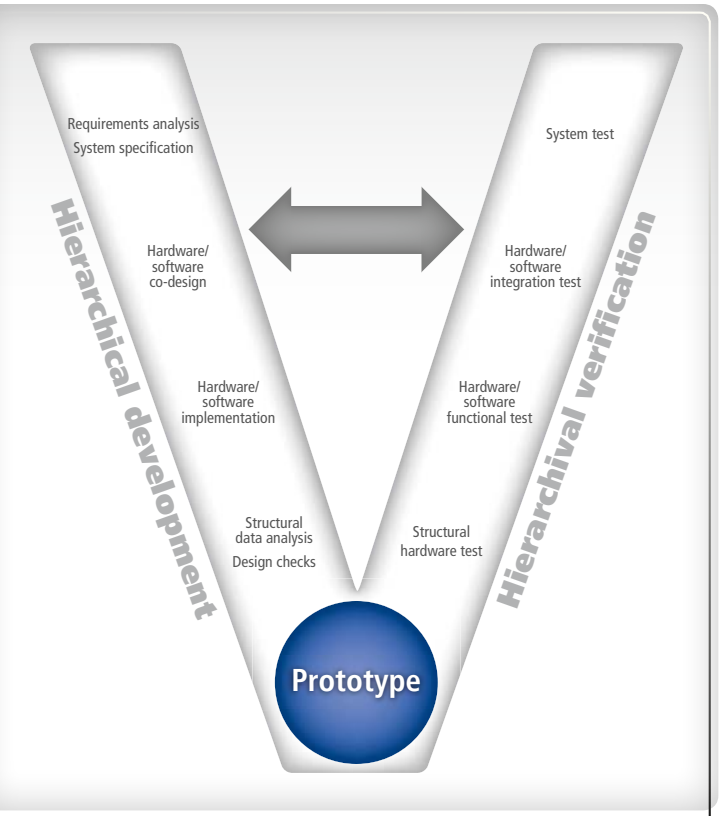
- hierarchical prototype development and validation
- pilot run production and testing
- field maintenance and repair of serial products.

All of these stages are based on their own processes and require **target-oriented applications**. In essence, the foundation for high product quality is already laid in the development labs.
The „**V-model**" plays a significant part in controlling increasingly complex designs. It defines adequate partial verifications for each hierarchical development stage by means of **specific test procedures**. These verifications include:

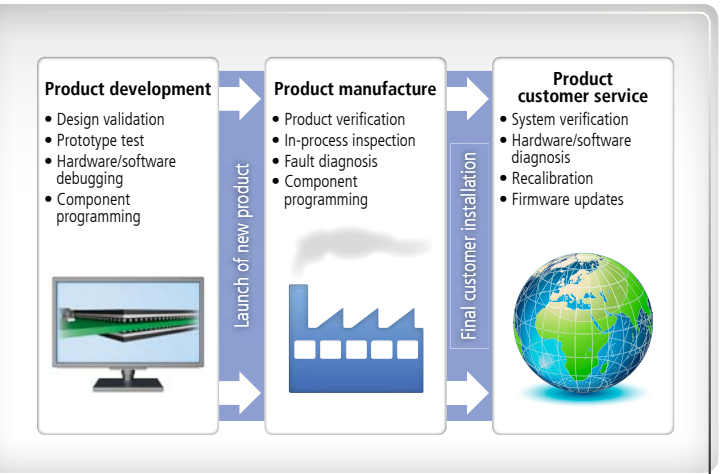
- structural tests (structural validation of the hardware)
- functional tests (functional validation of the modules)
- integration tests (interface validation of the modules)
- system tests (functional validation of the prototype)

In addition, parametric tests with firmware or hardware specifically programmed in part to optimise the prototype are typically performed in the course of these validations. This leads to a series of **other procedures** such as:

- performance tests (optimisation of the system performance)
- stress tests (optimisation of the system stability)
- reconfigurations (flash/PLD/MCU programming)



The **V-model** harmonises development and validation



Overview of a **product life cycle**

Even though the final objectives in the **individual stages of the product life cycle** differ, they use a number of essentially **identical** test and programming **applications**.

Feature	Laboratory	Production	Field
Objective	**marketable prototype**	**salable batch product**	**avalable system**
Test focus	• design error	• production error	• operating error
Optimisation criteria	• development period • validation quality • time-to-market • fast prototyping • reliability • testability	• fault coverage • test throughput • diagnosis quality • test costs • yield • repair costs	• diagnosis costs • repair time • repair costs • maintenance costs • calibration costs • MTTF/MTBF
Test processes	• structural test[1] • functional test • system test • integration test • performance test • stress test	• structural test[1] • functional test • system test • diagnosis test[2] • self-test[2] • HASS/HALT	• structural test[1] • functional test • system test • diagnosis test[2] • self-test[2] • remote test[2]
Debugging processes	• firmware • hardware	• hardware	• hardware • software[2]
Programming processes	• PLD/FPGA • flash memory • micro controller	• PLD/FPGA • flash memory • micro controller	• PLD/FPGA[2] • flash memory[2] • micro controller[2]

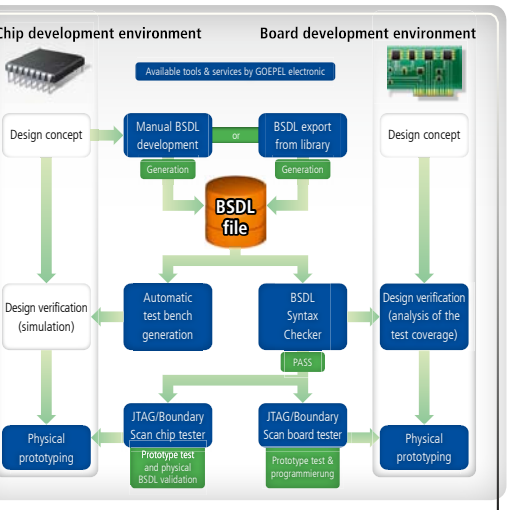
[1] via JTAG/Boundary Scan [2] requires Embedded System Access (ESA)

Access to the **unit under test** (UUT) in order to execute the desired application is **a key issue** in the case of all above mentioned processes. **Using the Embedded System Access** (ESA) offers the unique opportunity to use **standardised** multi-dimensional platforms for JTAG/Boundary Scan based instrumentation through **all product life cycle stages**, while **continuing to use** existing applications.

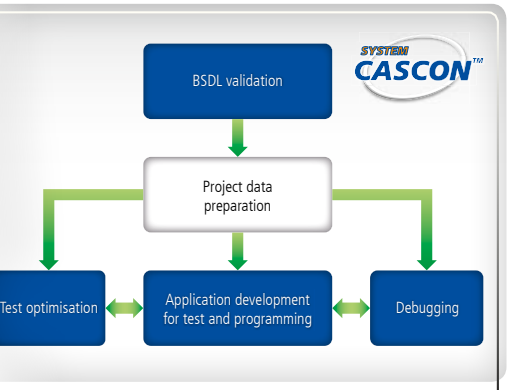
Further information on **Embedded System Access** technologies and our **products** is available at

goepel.com/**en/esa** goepel.com/**en/esa/instruments**

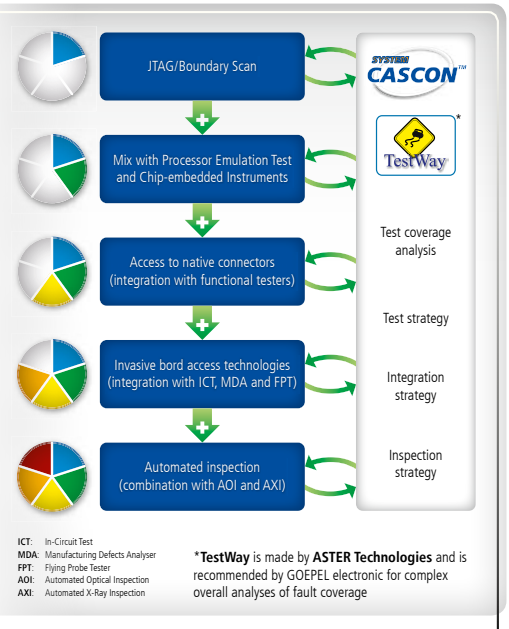
JTAG/Boundary Scan
The Proper Tool for Each Application



BSDL: connecting element between design and test



Workflow including debugging and test optimisation



Gradual optimisation of fault coverage

Keeping Track of the Entire Workflow

In addition to the **core process** for testing and programming, successful project development also requires a number of **supplementary processes** such as:

- BSDL validation
  (BSDL: Boundary Scan Description Language)
- Test program debugging
- Hardware debugging
- Optimisation of testability
- Optimisation of fault coverage

For these processes, too, we offer fully integrated support as part of the available hardware and software platforms, thus ensuring that the **entire workflow** can be covered **in a single system environment**.

Objective		Software/hardware
BSDL validation	• Syntax check • Semantics check • Techn bench generation for simulations • Physical verification of the BSDL file against the silicon	• TAP Checker • Syntax & Semantic Checker • ATPG/PFD Infrastructure • Device Checker Hardware TAP Checker™ SYSTEM CASCON™
Debugging	• Test program debugging • Pin toggling • Scan cell toggling • Data register watching • Data register loading • Waveform analysis • Network analysis • Instructions change • Circuit verification • Fault isolation • Pin status detection	• ScanAssist Interactive Pin-Toggler • ScanAssist Multi Mode Debugger • ScanVision Schematic • ScanVision Layout • ScanVision Virtual Schematic • Advanced Vector Browser • PicoTAP, SCANBOOSTER or SCANFLEX Controller SYSTEM CASCON™
Test optimisations	• Testability reviews • Optimisation of test coverage • Maximisation of throughput • Definition of the test strategy • Qualification of the integration strategy	• Design and Testability Explorer • Test Coverage Analyser • ScanVision Schematic • ScanVision Layout • ScanVision Virtual Schematic SYSTEM CASCON™

All processes are included in the principle of **graphic project development** on which the SYSTEM CASCON is based.
This is made possible by extremely powerful **visualisation tools**, such as **Mission Assist™** oder **ScanVision™**, which are fully integrated into the software platform. In addition, we offer a broad range of **ATE integration packages** and **automated inspection systems** aimed specifically at test optimisation.

Detailed information and datasheets on our **products** and **integration solutions** are available at
goepel.com/**en/esa/instruments** goepel.com/**en/esa/integration**

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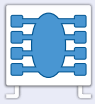
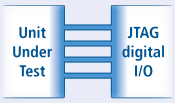
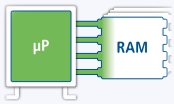
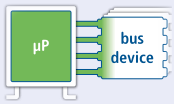
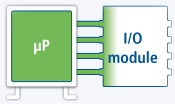
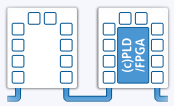
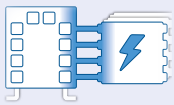
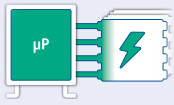
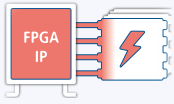
BST-AF/E/2012-04

Overview: Functional/Emulation Tests, Programming

Functional/ emulation tests	Test coverage	Speed[2]	Controller: PicoTAP	Controller: SCANBOOSTER	Controller: SCANFLEX	Required I/O modules	Required software tools
 Internal chip test	• Connections to core logic • Core functions	• static	●	●	●		• SVF Compiler CASCON
 Cluster test	• Connections to the cluster • Cluster functions • Connections within the cluster	• static	●	●	●		• ATPG Clusters (Waveform) • ATPG/PFD Clusters (Truth Table) CASCON
 Board I/O test	• Connectors • Peripheral I/Os • Board functions • Connections within boards • Simulated functions by means of DTIF* *(Digital Test Interchange Format, IEEE 1445)	• static • at-speed* *PXI or SCANFLEX I/O modules	●	●	●	• CION Modules • PXI I/O modules • SCANFLEX I/O modules	• ATPG/PFD IEEE 1445 (DTIF) • ATPG/PFD Clusters (Truth Table) • ATPG Clusters (Waveform) CASCON
 Core-assisted RAM access test	• SRAM connections • DRAM connections • DDR-SDRAM connections • Inline buffer	• at-speed			●		• AVTG[1] Dynamic Memory Access • PFD Memory Access • VarioTAP IP for micro processor CASCON VARIO TAP
 Core-assisted system bus test	• Bus connections • Write and read functions • Bus device functions • Board and system functions • Switches, LEDs, displays	• at-speed			●		• AVTG Bus Devices • PFD Clusters (Truth Table) • VarioTAP IP for micro processor CASCON VARIO TAP
 Core-assisted I/O test	• Analog and digital I/Os • Communication bus interface • Actuators, sensors • System bus interface	• at-speed • real time			●	• CION Modules • PXI I/O modules • SCANFLEX I/O modules including Bus Acces Cables • ICT[1]/FPT[1]/FCT[1] channels	• AVTG Bus Devices • Basic VarioTAP Test Generation • VarioTAP IP for micro processor CASCON VARIO TAP

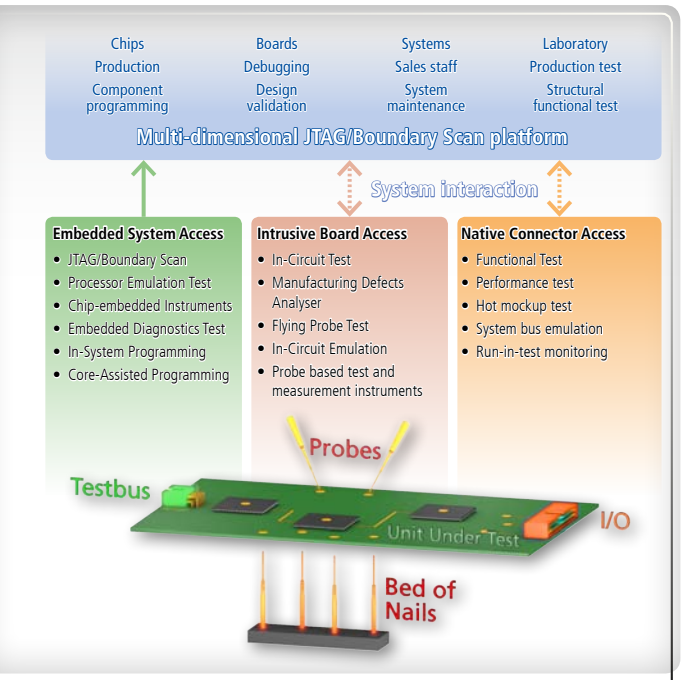
Boundary Scan methods **Processor Emulation Test**

[1] **AVTG**: Automated VarioTAP Test Generator • **ICT**: In-Circuit Tester • **FPT**: Flying Probe Tester • **FCT**: Functional Tester
[2] **Speeds**: real time > at-speed > static

Programming of components	Test coverage	Speed[2]	Controller: PicoTAP	Controller: SCANBOOSTER	Controller: SCANFLEX	Required I/O modules	Required software tools
 PLD/FPGA programming	• Programmable Logic Device (PLDs) • Field Programmable Gate Arrays (FPGAs)	• Depends on the controller	●*	●*	●		• PLD Program Generators CASCON
			*limited performance in part				
 Boundary Scan flash programming	• Parallel NAND flash memory • Parallel NOR flash memory • Serial flash memory (I²C, SPI) • Electronic multimedia cards • Phase-change memory	• Low to medium Recommended: high-speed programming via VarioTAP or ChipVORX	●*	●*	●		• Automated Flash ISP (AFPG) CASCON
			*suitable for small data volumes				
 Micro controller programming	• On-chip flash of micro controllers (MCU)	• High-speed up to turbo-speed* *if flash image transfer via LAN is availabe			●	• SCANFLEX I/O modules including Bus Acces Cables Option for flash image transfer via LAN	• Automated VarioTAP Flash ISP (AFPG) • VarioTAP IP for micro processor CASCON VARIO TAP
 Core-assisted flash programming	• Parallel NAND flash memory • Parallel NOR flash memory • Serial flash memory (I²C, SPI) • Embedded multimedia card (eMMC) • Phase-change memory	• High-speed up to turbo-speed* *if flash image transfer via LAN is availabe			●	• SCANFLEX I/O modules including Bus Acces Cables Option for flash image transfer via LAN	• Automated VarioTAP Flash ISP (AFPG) • ChipVORX IP CASCON VARIO TAP
 FPGA-assisted flash programming	• Parallel NAND flash memory • Parallel NOR flash memory • Serial flash memory (I²C, SPI) • FPGA boot flash • Phase-change memory	• High-speed up to turbo-speed*			●		• Automated Flash ISP (AFPG) • ChipVORX IP CASCON CHIP VORX

Boundary Scan methods **Core-assisted Programming** **FPGA-assisted Programming**

Applications Based on Embedded System Access (ESA)



Correlation between application, instrumentation and access

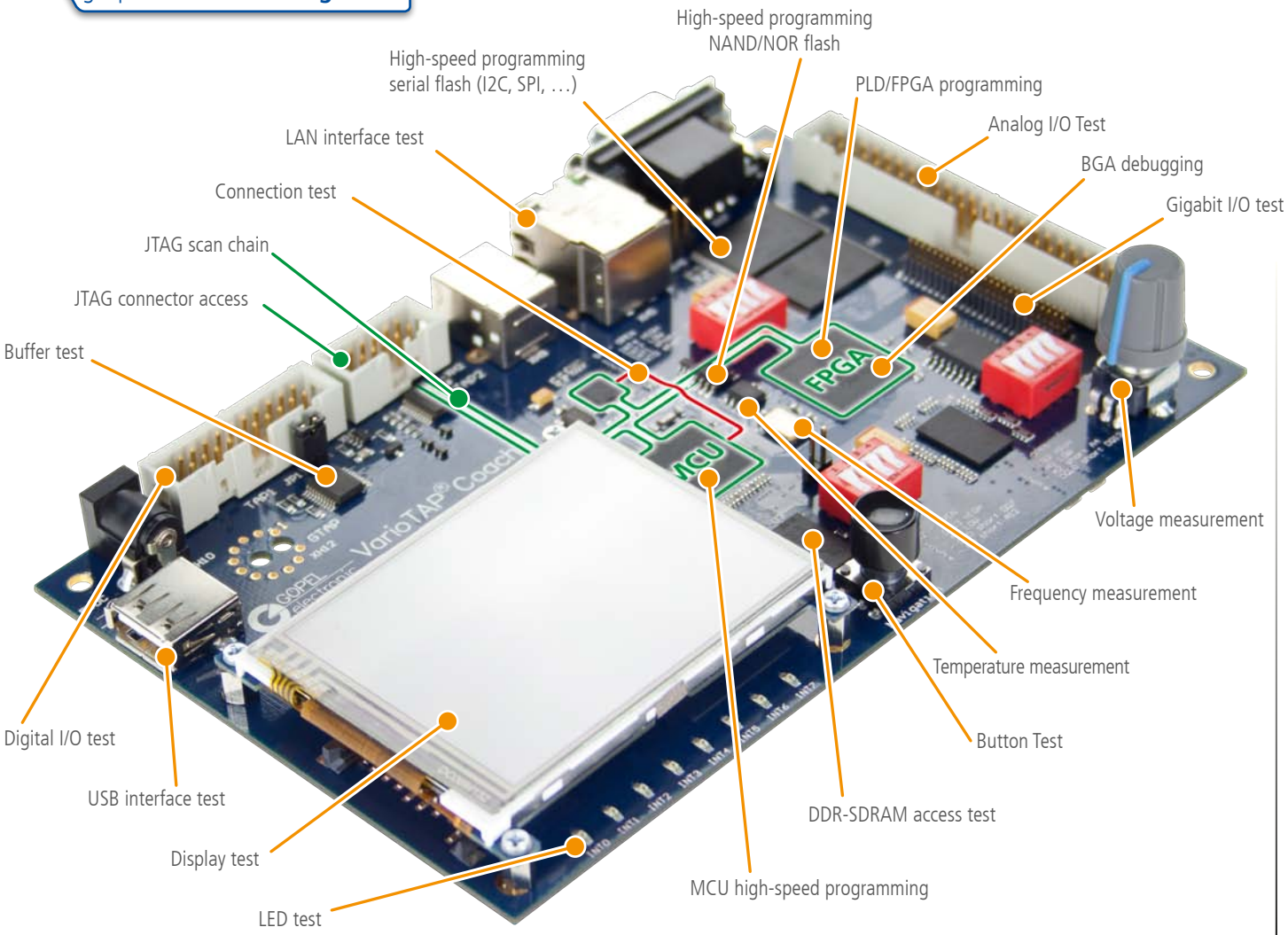
Classification of Target Applications

Each application pursues certain **basic objectives**, such as testing, programming, debugging or validation, and is defined by certain very specific characteristics, such as execution speed, execution environment or interaction with other instruments. In this context, the **following application types** are especially important for **Embedded System Access (ESA)**.

Application type	Key application contents
Structural test	Checking the proper connection between the various circuitry elements
Functional test	Checking the proper functioning of ICs, clusters, boards, interfaces and systems
Emulation test	Test conducted by the micro processor through emulation (special instance of functional test)
At-speed test	Execution: structural, functional or emulation test at higher speed
Real time test	Execution: structural, functional or emulation test at nominal speed
Analog measurement	Measurement of voltage, frequency, temperature, waveform
Debugging	Interactive test of individual registers, pins, connections or logic functions
Programming	Programming of non-volatile memory (flash, micro controller, PLD)

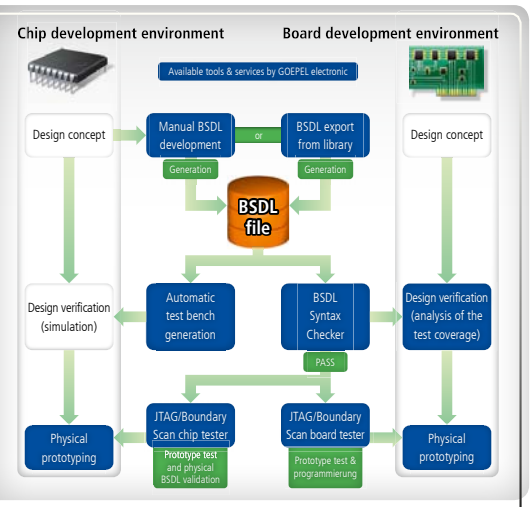
Our multi-dimensional JTAG/Boundary Scan platform **supports** not only **all** of the above mentioned **applications**, but also offers the option to interactively combine other access methods through open system integration. In this way, we are able to provide a flexible and **universally deployable solution**.

Further information on **test strategies** and **system integration** is available at
goepel.com/**en/esa/integration**

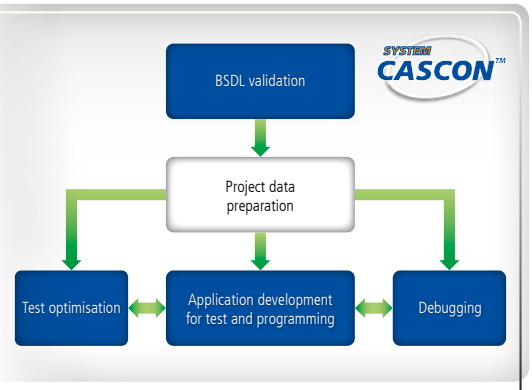


Practical **examples** of applications based on **Embedded System Access** technologies

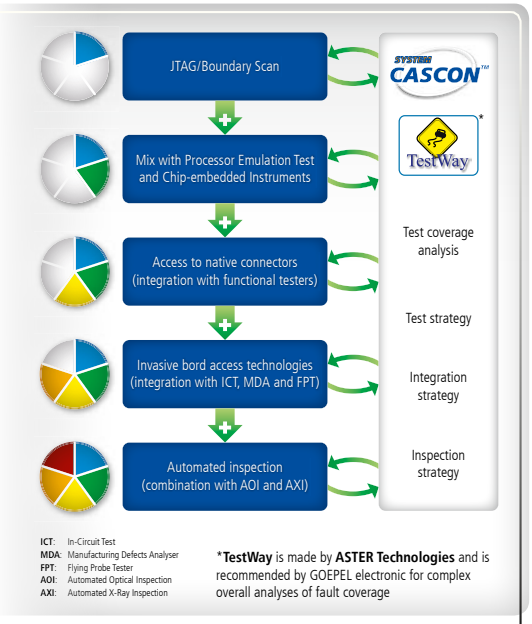
The Proper Tool for Each Application



BSDL: connecting element between design and test



Workflow including debugging and test optimisation



Gradual optimisation of fault coverage

Keeping Track of the Entire Workflow

In addition to the **core process** for testing and programming, successful project development also requires a number of **supplementary processes** such as:

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  (BSDL: Boundary Scan Description Language)
- Test program debugging
- Hardware debugging
- Optimisation of testability
- Optimisation of fault coverage

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