TestWay Express®

Lean NPI optimizes Test Coverage

TestWay Express is a fully integrated solution that enables electronic manufacturers to optimize the design to test flow:

- Define the manufacturing line; including a combination of assembly, inspection and test machines.
- Estimate the test coverage of each individual stage and optimize the combined results.
- Generate the input files for each test stage that reflect the selected strategy.
- Measure the real test coverage by importing the post-debug test program or coverage data.
- Compare the early estimation with the actual measured test program coverage, identifying gaps in the overall strategy.

Test is essential for improving product quality by striving to detect and prevent all faults on a product. This maximizes the number of good products shipped to the customer. It is important to:

- Define the optimum test strategy to maximize the test coverage.
- Produce a test specification document that defines what to test.
- Compare the developed tests against the test requirements.
- Understand the production process capability and determine an acceptable level of defects that can be shipped to the customer.

TestWay Express analyzes the number of defects detected at each stage in the test process and identifies any shortfall in test coverage and undetected defects. It allows the computation of the IPC metrics such as first pass yield (FPY), fall-of-rate or escape rate by importing the real time DPMO (Defect Per Million Opportunities) from the manufacturing process. The manufacturing test strategy is tuned to provide the optimal test coverage for identifying potential defects.

TestWay Express is built around **TestWay**, the industry leading DfT and test coverage analysis tool from the ASTER product portfolio.

EASE OF USE

A combination of application wizards, and drag and drop operations guide you through the project creation to enable coverage reports to be generated in **6 easy steps**:

- Input the board data.
- Modelize the components.
- Place the probes.
- Select the manufacturing strategy
- Generate input files for test & inspection machines.
- Create the test coverage reports.

Key product benefits:

- **Ease of Use**
  Application wizards guide you through the project. Add multiple test strategies for project analysis, by simply drag and drop from the machine list.

- **Probe allocation & accessibility**
  Place probes aligned to priority rules for top or bottom side access using test points, connectors, vias, THT, SMD, bead probes, and generate detailed accessibility report.

- **Test coverage estimation**
  Maximize test and inspection coverage by estimating coverage aligned to selected test strategies. Perform "what-if" analysis to select the optimal test strategy, to achieve maximum coverage.
  Eliminate redundant test steps.

- **Automated test program creation**
  Generate the input files for AOI, AXI, BST, ICT, FPT in a matter of minutes or hours rather than days.

- **Test coverage measurement**
  Determine the real test coverage and compare against the early estimation to identify areas for improvement.

- **Yield estimation**
  Calculate the first pass yield (FPY) by importing real time DPMO data for the manufacturing process to tune the test strategy for optimum test coverage.

- **Wide variety of testers supported**
  Import & Export test programs from a wide range of vendors, more than 45 test & inspection machines supported.

- **Layout from native CAD formats**
  Create layout view from standard CAD formats such as GENCAD, CAMCAD, FATF, ODB++, or direct from native CAD layout data.

- **Component classification**
  Visualize and edit component attributes such as part number, shape, class, value, tolerance, mounted status, etc.
  Prompts for missing information.

INPUT BOARD DATA

53 CAD importers are available to support layout, schematic netlist and schematic graphics. This is a key differentiator as other commercial DfT tools work only from the layout stage. **TestWay Express** operates from native CAD formats and ensures the full interoperability between all stages across the design/manufacturing flow.
CAD data is required to understand the board design. Geometrical and electrical information such as component class, value, tolerance, package shape, height, centroid and test probes are automatically extracted.

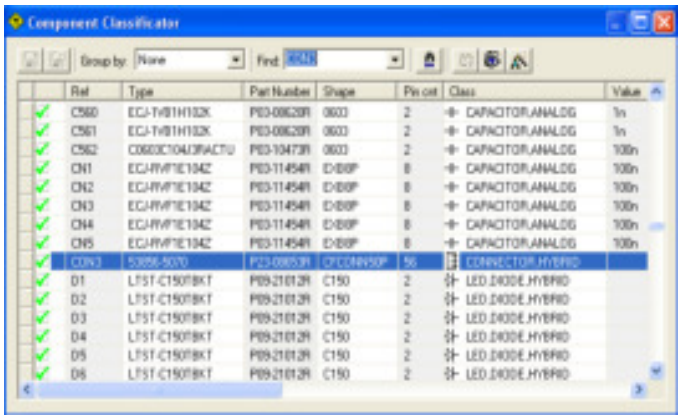
The probe locations are referenced when assessing the nodal access for flying probe and in-circuit during test program generation or coverage analysis.

The Bill Of Material (BOM) can be used to supplement the CAD data with additional attributes that may not be provided in the CAD data, such as part number, component description, value, mounted status, etc.

The board schematic can be imported to allow full interaction between the reports and the viewer, and to visualize any attributes such as test coverage.

MODELIZE THE COMPONENTS

The better the components are modelized, the more accurate is the test strategy analysis.



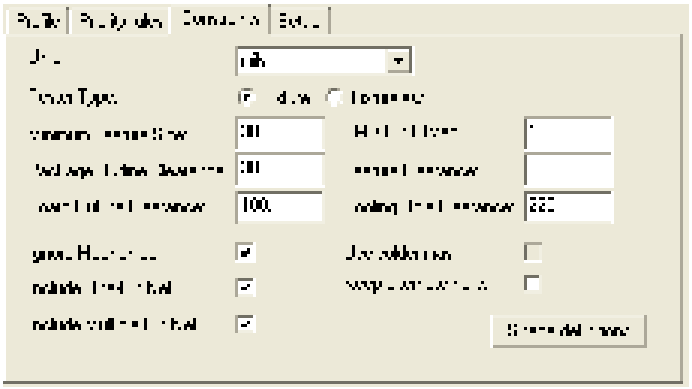
The component classificator is a user friendly editor that allows users to:

- Edit component type, value, tolerances, part number, etc, which is required to determine the type of test that can be conducted on the component.
- Define pin function of polarized components and internal component structures for multi-element components such as resistor packs or double diodes.
- Import BSDL file to describe the boundary-scan cell structure of boundary-scan compliant devices.
- Re-use IBIS, TestWay or test models in order to specify component and pin attributes.

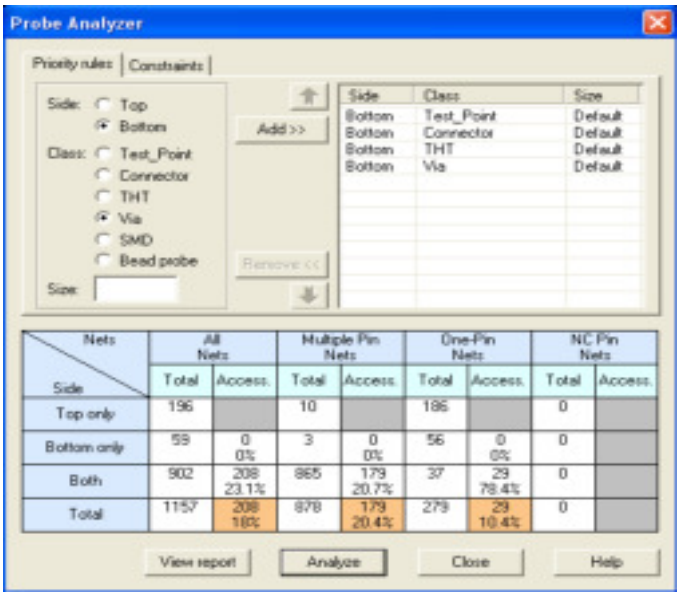
A component wizard is provided to simplify the component modeling by automatically identifying device classes, importing any available models and extracting valuable component information such as value, tolerance, shape etc, directly from the BOM description.

PLACE THE PROBES

Probes are placed by considering the mechanical and design for test (DFT) constraints practiced by respective companies.



Probe locations may already be defined within the CAD data, but there may be insufficient access for total test coverage. In which case the probe analyzer can be used to consider alternative top and bottom side accessibility options such as through hole pins (THT), connectors, SMD pads, vias or bead probes etc.



Once the possible probe positions have been analyzed, the nail allocation algorithm selects the best of these opportunities for the nail positioning according to the preferences set by the user.

This allows the estimated coverage to be calculated according to the real test access.

TestWay Express generates a complete set of documentation:

- Accessibility report is created to provide a list of the nodes that do not have access, with reference to the rule placement violation that prevents access.
- Check plots and drill files.
- List of probes and nails in MS-EXCEL format.
- Nail retro-annotation back to the schematic. This is helpful for repair because it allows visualization of nails on the layout, schematic and virtual schematic viewers with full cross-probing.

SELECT MANUFACTURING STRATEGY

When deciding on the optimal test flow, it is important to consider all available test and inspection machines such as AOI, AXI, BST, ICT, FPT and Functional test.

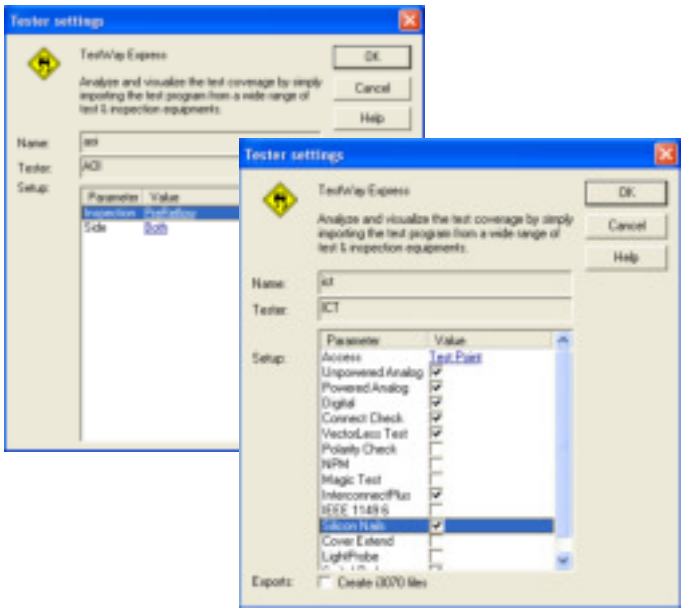
The “test line” is easily defined using a simple drag and drop operation. The theoretical test models for coverage estimation and the actual test models for coverage measurement, can be combined to reflect your manufacturing strategy.

The gauges provide a quick view of the level of component modeling and board accessibility. To review the respective report, you simply click-on the gauges !

COVERAGE ESTIMATION

Each of the theoretical test strategies allows selection of tester settings from a feature list for a particular test strategy.

In order to provide a more accurate estimation, any specific test features that are available on the target tester should also be included in the analysis. This aligns the estimated coverage to the real tester coverage.



TestWay Express handles cross optimization along the test line such as Boundary-Scan or AOI that can be used to minimize the In-Circuit Test or Flying Probe Test.

DESIGN TO TEST

The test strategies simulation results are used to automate the assembly, test & inspection program generation for assembly machine, in-circuit test (ICT), flying-probe, X-ray, Automated Optical Inspection (AOI) and Boundary-Scan test. Output processors are available for test & inspection machines from leading suppliers such as Acculogic, Aeroflex, Agilent, Asset, Goepel Electronics, JTAG Technologies, Takaya, Teradyne/Genrad, Mydata, XJTAG and ...
In addition to creating the test machine input files, TestWay Express also generates test models for analog multi-element components and digital models including disable configuration.

REAL COVERAGE

The real test coverage is determined after the test has been developed and debugged, by analyzing the test program or coverage reports from a wide range of test and inspection systems used within the industry.

Industry standard coverage metrics such as PPVS (Presence, Polarity, Value, Solder), or PCOLA/SOQ (Placement, Correct, Orientation, Live, Alignment / Short, Open, Quality) are used in calculating both the estimated and real coverage, so that the same analysis criteria is used in the overall analysis.

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More than 45 coverage importers are available from the leading test and inspection suppliers within the industry.

When combining theoretical tester models with the real tester program, or report. It allows direct comparison to verify that the completed test program is in alignment with your early expectations.

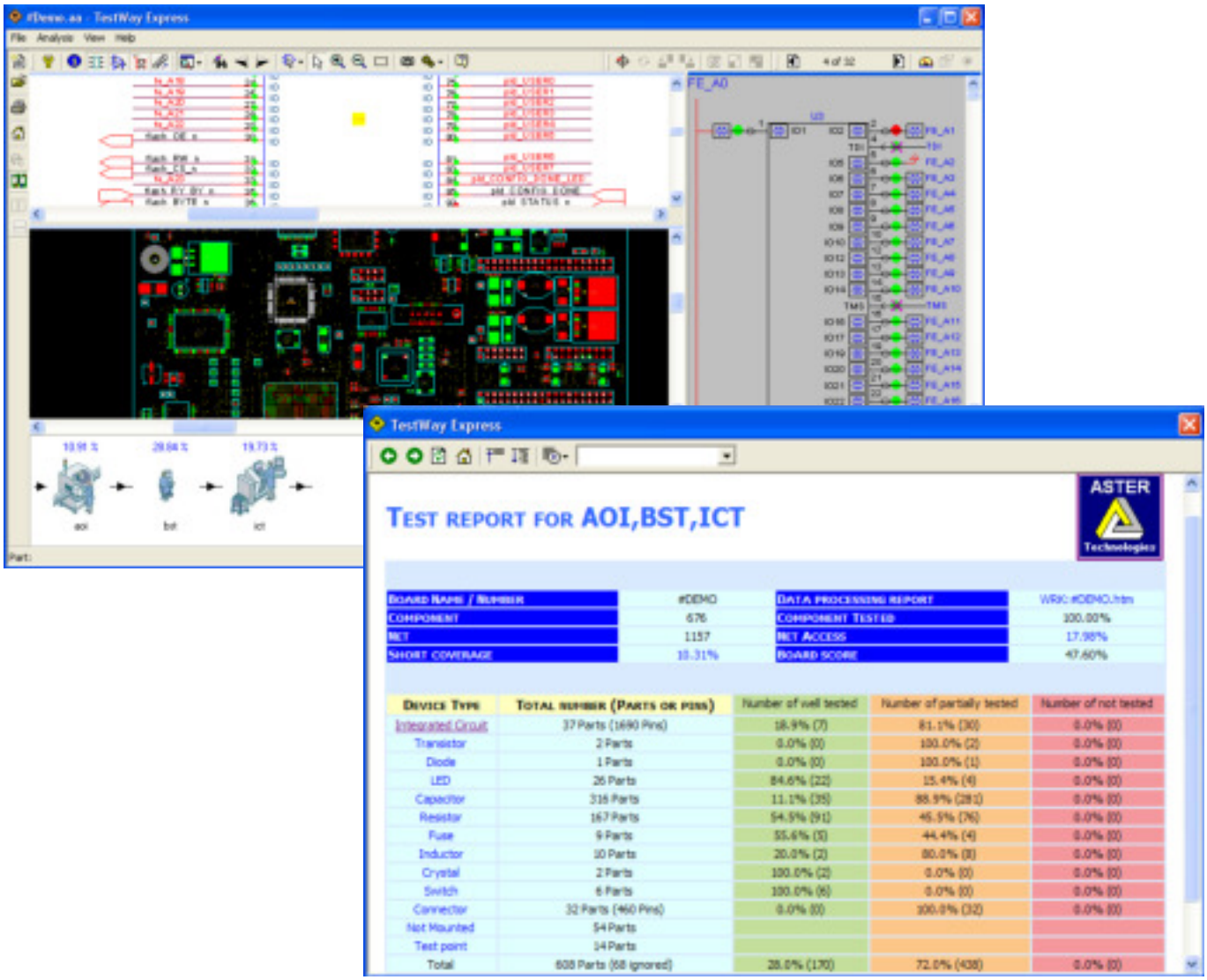
EXPLORE TEST COVERAGE

Once the test strategy is defined and the respective tester settings are selected, simply press the “Analyze” button to launch the analysis and visualize the resultant coverage across all views and reports.

TestWay Express creates a variety of comprehensive HTML and MS-Excel reports.

- Board level overview of the combined coverage, or independent reports that define the coverage provided by each of the test and inspection machines in the test line.
- All components are categorized within the “Device Type” field. To access the pin level coverage simply select the device category to drill down to the component list and select the respective device.
- The overall coverage is defined by the “board score” within the top level report. The individual coverage scores for the respective test strategies are highlighted in the test line.
  Individual test reports can be viewed by selecting the respective tester from the test line.
- Navigation is aided by full interactive cross-probing between all the HTML reports, the schematic, layout and virtual schematic views.
- Coverage visualizations are categorized using easy to interpret traffic light color coding.

Not tested
Partially tested
Well tested



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