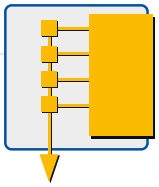
White Paper

VarioTAP®



Thomas Wenzel / Heiko Ehrenberg

Combining Boundary Scan and JTAG Emulation for Advanced Structural Test and Diagnostics

GOEPEL electronic
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New Challenges in Test

While continuously improving IC and SOC technologies, higher clock rates, and more powerful processors are music to the design engineers' ears, the headaches of test engineers are getting worse and worse. This is hardly surprising. As the ever decreasing test access was the worrying factor in the past, a new problem arose in recent years in the dramatically increasing speed of the signal transmission and the dynamic of associated functions. The resulting failure phenomena and test access limitations have an inevitable impact on the efficiency and practicality of test strategies. **Table 1** shows a qualitative comparison of various electrical test methods, and illustrates trends.

It is apparent that structural tests (detecting connectivity faults, such as open pins, solder bridges / shorts) have huge advantages regarding test automation, diagnosis, and deterministic fault coverage. However, test coverage for dynamic failure phenomena demands higher test speed in order to carry out at-speed tests. For this, functional tests are more suitable, although test development effort is enormous and failure diagnosis is rather limited. A single test technique that meets all requirements is neither existent nor on the horizon. Instead a suitable mix of techniques is the way to go. The combination of Boundary Scan and emulation test can be considered as a particularly interesting approach.

Feature	Electrical Test Technology				
	FPT	ICT	FCT	BST	Ideal
Test method and access technique to UUT	structural probes	structural fixed nails	functional connectors	structural scan cells	non invasive
Automation level for Test Generation / Fault isolation	high	high	low	high	high
Typical fault coverage and typical test frequency	analog static	high <10 MHz	high at speed	digital static	high at speed
BGA Pin access quality and trend for future designs	low declining	low declining	very low no change	high increasing	high increasing
Test implementation costs and effort for future use	raising	critical level	low	low	low
Typical test throughput and scalability of ATE platform	limited	high	high	high	high

Table 1

Boundary Scan and Emulation Test – Friends or Foes?

The basic idea of Emulation tests is not new; in fact, it was successfully used and supported with device-specific tools since the early 1980s [1]. Processor specific Pods, inserted into the Device Under Test's (DUT) socket instead of the actual device (e.g. a µP), were used to take over control of the Printed Circuit Assembly's (PCA's) system bus. Respective bus emulation tests provide testability of all connected components, including peripheral interfaces. The same technique was also used for software verification in the form of In-Circuit-Emulators (ICE).

However, decreasing physical access and increasing clock rates called for new concepts. Today, device emulation is done with on-chip emulation circuitry, also known as On-Chip Emulators (OCE). Besides proprietary interfaces, the JTAG Test Access Port (TAP) defined in IEEE Std. 1149.1 is often applied as a communication port. Another standard defines a debug interface [2] utilising the TAP, however, in practice we can find various implementations of JTAG emulation ports. The fascinating aspect of this solution is that the DUT (e.g. µP) core can be controlled over just 5 wires, potentially without any additional external hardware resources, and without loss of performance. This benefit can be exploited in JTAG TAP controlled emulation tests. **Figure 1** shows how such an Emulation Test compares to standard Boundary Scan tests.

The comparison shows the complementary character of both techniques. Emulation Tests can be considered as classic Functional Tests, and therefore have the same advantages and disadvantages. A combination of both techniques—Boundary Scan and Emulation Test—seems absolutely reasonable, however respective system solutions must exploit the synergy between both methods. In this regard, GOEPEL electronics' VarioTAP® technology offers new possibilities.

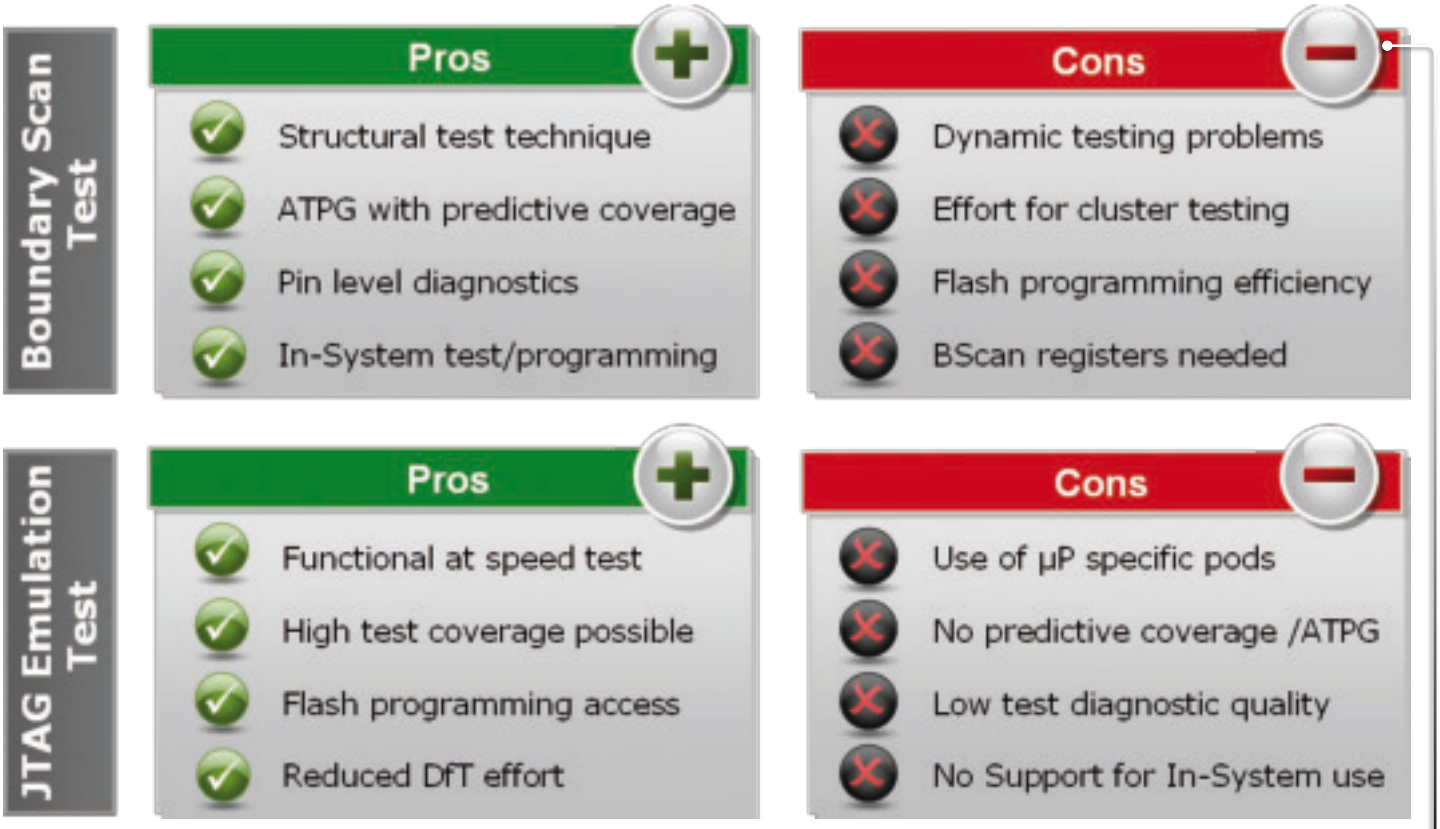


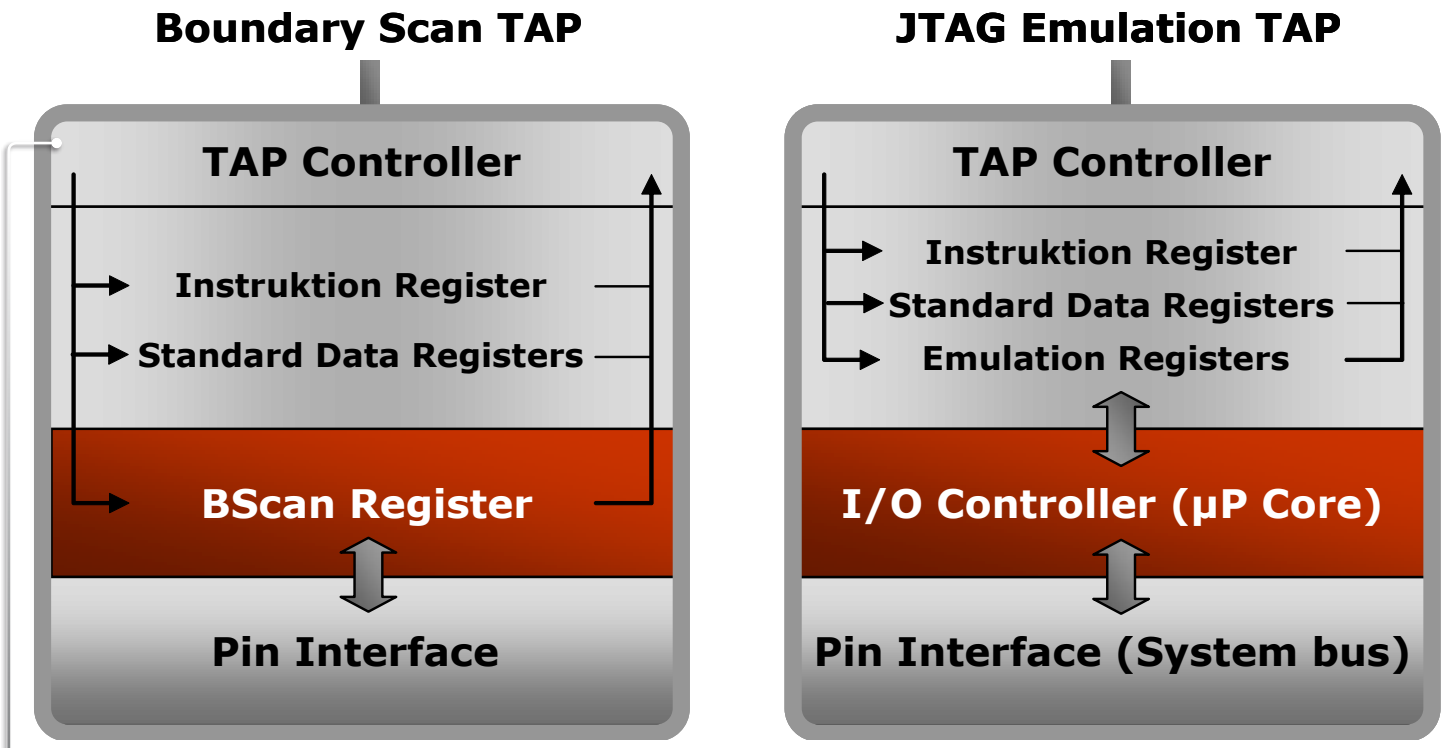
Figure 1 - Comparison of basic advantages and disadvantages between Boundary Scan and traditional JTAG Emulation Test

VarioTAP® – Fusion of Boundary Scan and Emulation Test

An examination of previously available system solutions involving Boundary Scan and Emulation Test leads to classification in three performance classes [3]:

- Loose combination
- Hybrid integration
- Total fusion

The first two classes differ particularly in the capability (or lack thereof) to use consistent hardware and software for the test execution. I.e. a loose combination of Boundary Scan and Emulation Test tools requires separate hardware and software tools (typically device specific software and JTAG pods are required for Emulation Test), while a hybrid integration can utilise the same JTAG controller hardware, and possibly even the same software, for both Boundary Scan and Emulation Test. The test generation for Boundary Scan and Emulation Tests, however, is carried out separately, in both classes. Therefore, the potential of each method is not fully taken advantage of, since a Boundary Scan test will not become more dynamic, nor will an Emulation Test become more structural or provide better diagnostics. VarioTAP® on the other hand, as the first representative of the third category, views Emulation Test from the same perspective as Boundary Scan, providing test access utilising design integrated pin electronics (**Figure 2**). With this approach, the VarioTAP® software tools allow the control of dynamic emulation pin electronics at the same vector level as static Boundary Scan pin electronics. Hence, the handling of Emulation tests seamlessly merges with the familiar handling of Boundary Scan tests, allowing direct interactions between Boundary Scan and Emulation Test as one element of the complete fusion (**Figure 3**).



- Static pin electronics
- BScan cells define vectors
- Serially controlled pin interface
- Scalable number of pins
- Arbitrary static signal timing
- Arbitrary vector definition per pin

- Dynamic pin electronics
- µP defines vectors
- Parallel controlled pin interface
- Fixed number of pins
- Rigid dynamic signal timing
- Vector definitions only possible for address and data bus

Figure 2 - Comparison of device (chip) internal architectures for pin access, Boundary Scan vs. JTAG based Emulation Test

The second element enabling this fusion is the adaptive streaming technology of VarioTAP®, allowing simultaneous control of both types of pin electronics (**Figure 4**). With the available tool suite for Automatic VarioTAP® Test Program Generation (AVTG), predictable fault coverage and pin level diagnostics is possible (in addition, VarioTAP® applications can be written manually in the programming language CASLAN). The AVTG tool for Memory Access Test, for example, uses structural test vectors and associated diagnostics similar to Boundary Scan based Memory Cluster Tests for the dynamic test of (dynamic high-speed) RAM. In this manner, a total fusion of Boundary Scan and Emulation test is achieved on the basis of a uniform software and hardware platform, paving the way for the application of advanced structural test strategies.

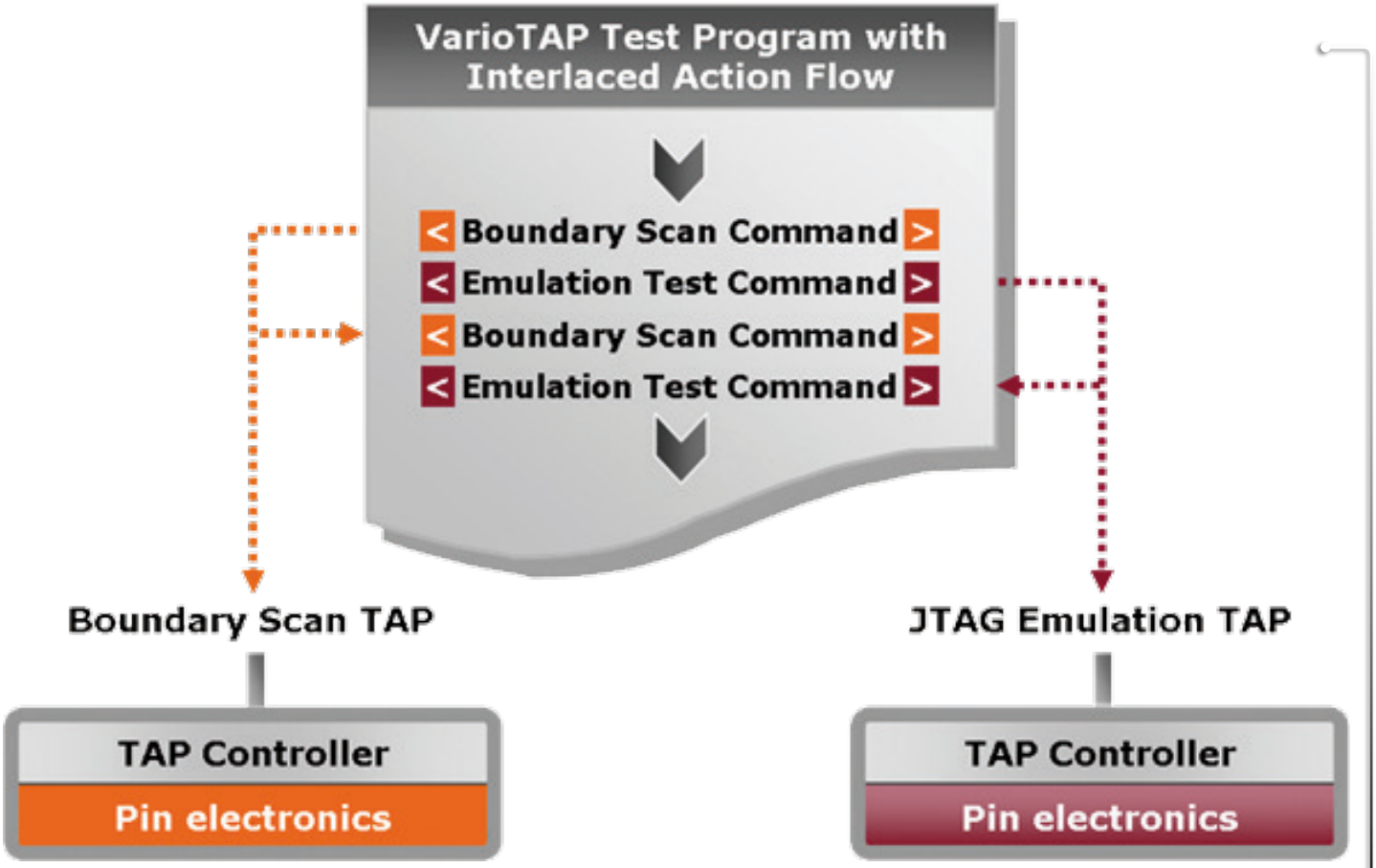


Figure 3 - Handling of Emulation Test operations at the same level as Boundary Scan operations

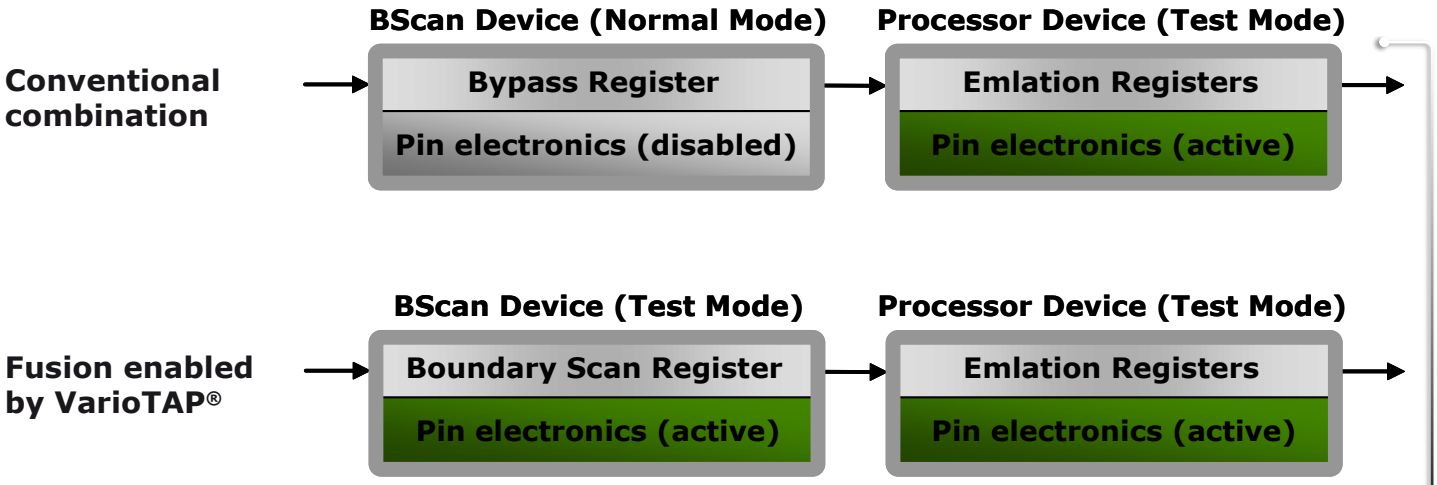


Figure 4 - Comparison of pin electronics usage for Boundary Scan and JTAG based Emulation Test in conventional combination vs. VarioTAP®

Teamwork clears the hurdles

Emulation Test via VarioTAP® extends the test coverage for modern designs significantly beyond what can be achieved with pure Boundary Scan (**Figure 5**).

At the same time, VarioTAP® simplifies some critical DfT (Design for Test) requirements such as clock controllability and enables fast Flash programming. Emulation Test is very effective and can fundamentally improve the quality of test, especially for testing highly complex non-scanable analogue and digital circuitry, as well as highly dynamic structures (**Figure 6**).

As a result, VarioTAP® overcomes in principle the limitations listed in **Figure 1** both for Boundary Scan and for conventional Emulation Test.

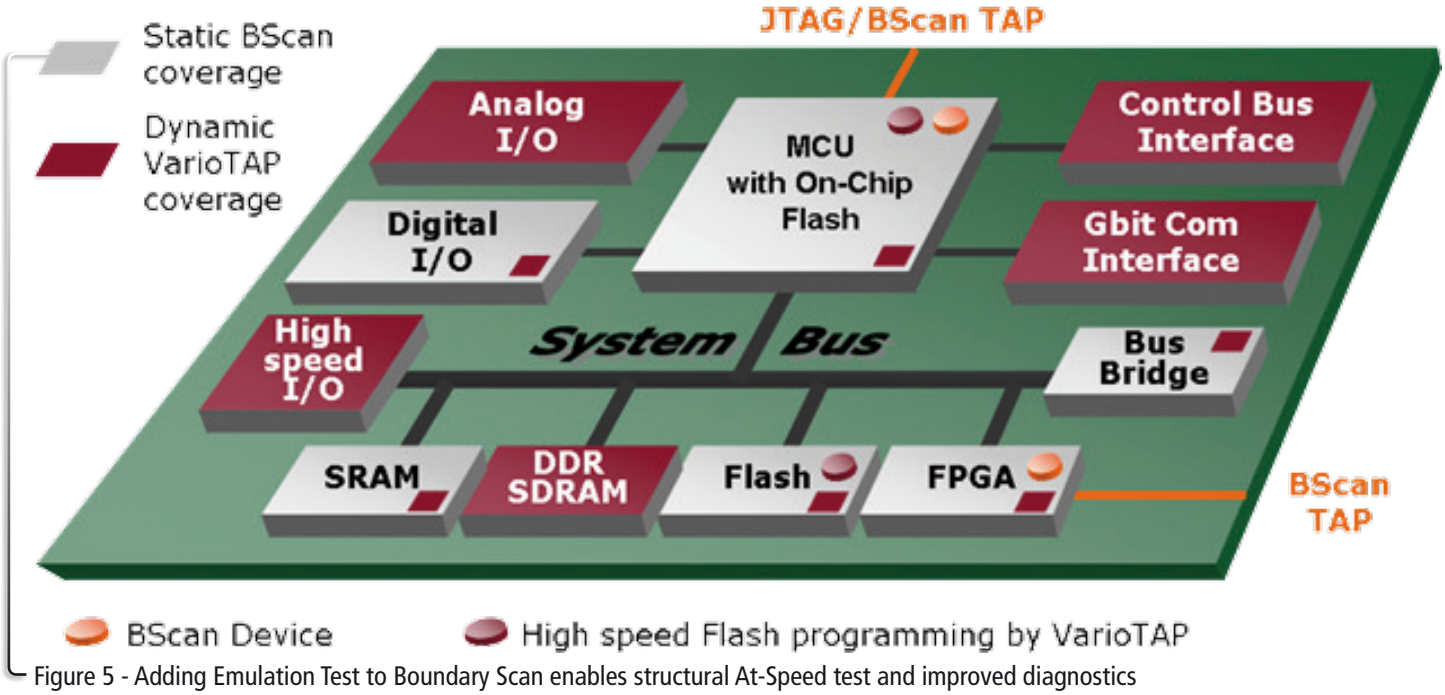


Figure 5 - Adding Emulation Test to Boundary Scan enables structural At-Speed test and improved diagnostics

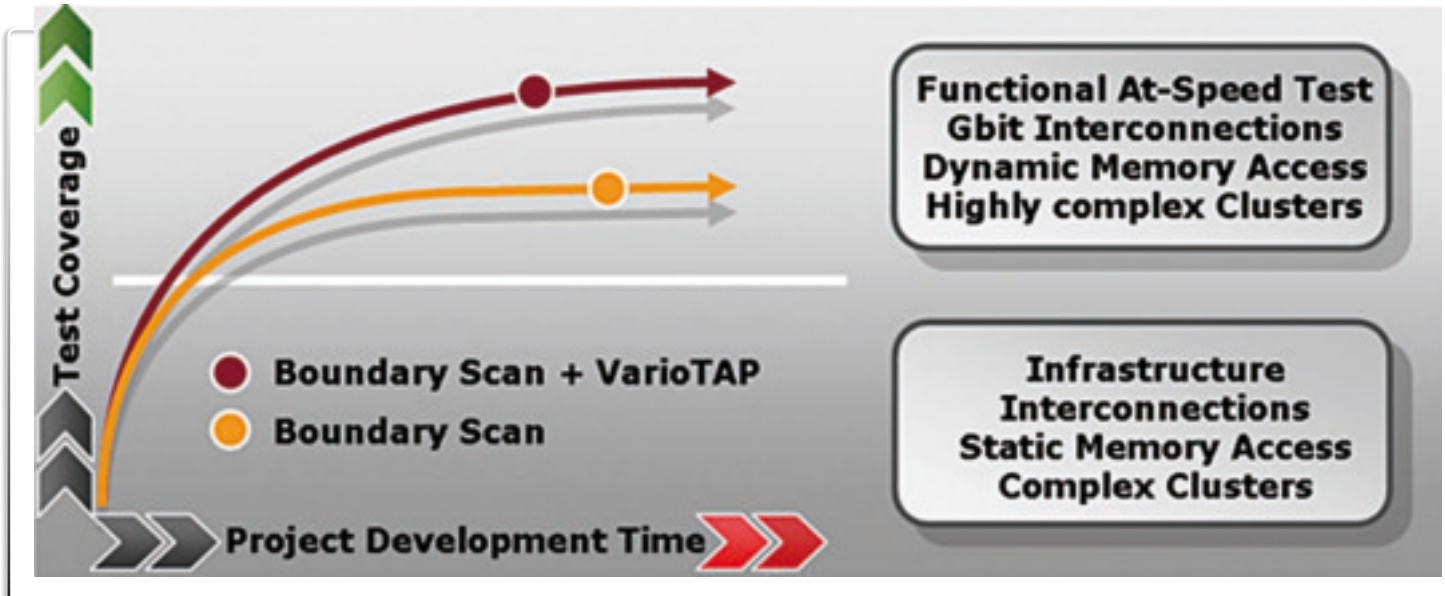


Figure 6 - Significant improvement of the test program quality with higher fault coverage and shorter development time

Ground-breaking benefits provided by VarioTAP®

Based on the previously mentioned technical features and the fact that VarioTAP® can interact not only with Boundary Scan but also with external test instruments, we see a multitude of essential benefits and new opportunities:

- Deterministic test coverage aids definition of optimal test strategies
- Highest productivity with automated test program generation
- Advanced structural test with pin level diagnosis
- No device-specific diagnostics software or firmware needed
- Uniform system platform with fully integrated tool suite
- Single language for control of both Emulation test and Boundary Scan test
- Simultaneous debugging of Boundary Scan and Emulation vectors
- Support for devices featuring on-chip emulation by VarioTAP® model library
- Fast programming of embedded or external Flash memory
- Multi-TAP and multi-core support including in-system emulation
- No need for device specific knowledge or tool chain
- Applicable as stand-alone system or integrated in ICT, FPT, MDA, FCT

As VarioTAP® does not require invasive test probes and is controlled only via the TAP signals, it can be utilised throughout the whole product life cycle.

- Prototypes can be tested faster and more exhaustive (Rapid Prototyping)
- Software developers can save the time to write special diagnostic routines
- Concurrent engineering of design and test is possible
- Allows hierarchical test at the SoC, board, and system level
- Cycle time for New Product Introductions (NPI) can be reduced
- Production tests provide better test coverage and become more cost-efficient
- Fewer test points and probes needed for ICT reduce fixture costs
- Shorter repair times due to improved diagnostics
- Lower "bone pile" with "dead" or "No Failure Found" boards
- Higher efficiency of field service applications

While stand-alone test systems are widely used in test labs, a mix of different test techniques is still recommended for the production environment. Various aspects need to be considered when defining a suitable test strategy (**Table 2**).
One of the most interesting strategies is the combination of Boundary Scan and VarioTAP® with Flying Probe Testers. The Flying Probe Tester can test the analogue circuitry, and then Boundary Scan / VarioTAP® can utilise the probes as virtual Boundary Scan pin(s) for the extended Boundary Scan tests and for more precise diagnosis [4].

Feature	Electrical Test Strategy			
	BST	BST +VarioTAP	FPT+BST +VarioTAP	ICT+BST +VarioTAP
Predictive coverage calculation	yes	yes	yes	yes
Structural Test coverage	high	high	Very high	Very high
Functional Test coverage	static	high	high	high
Test Program Generation	ATPG	ATPG	ATPG	ATPG
Diagnostics Quality	high	high	very high	high
Test access problems by nails	Not needed	Not needed	medium	high
Test of analog components	Very limited	Very limited	excellent	excellent
Fixture cost	low	low	low	high
Investments / cost of ownership	+	+	+++	++++

Table 2

A look at the implementation of VarioTAP® in SYSTEM CASCON™

VarioTAP® is completely integrated in the development environment SYSTEM CASCON™ (**Figure 7**).

Hence, the development of Emulation tests is based on the same project data that is used for Boundary Scan, with access to the same auxiliary tools, such as device library, multi-mode debugger, test coverage analyser, or ScanVision (for the graphical display of layout or schematic features, or visualisation of detected faults, for instance). In addition to the VarioTAP® tools, one element plays a crucial role - the VarioTAP® model. These models are structured as modular Intellectual Property (IP) and provide a behavioural definition of certain µP functions used in different VarioTAP® applications. We differentiate the following VarioTAP® applications: Flash programming, Bus Emulation Test (BET), and System Emulation Test (SET). Essentially, respective device models are to VarioTAP® what a BSDL file is to Boundary Scan (**Figure 8**).

The number of IPs, including custom IP, in a single VarioTAP® model is not limited. Furthermore, it is possible to simultaneously control several different Micro Controller Units (MCUs) on a Unit Under Test (UUT), since multiple VarioTAP® models can be active at the same time. On the tester hardware side, GOEPEL electronic's SCANFLEX® platform provides up to 8 independent TAPs. In the case of multi-core applications, the number of cores is theoretically unlimited.

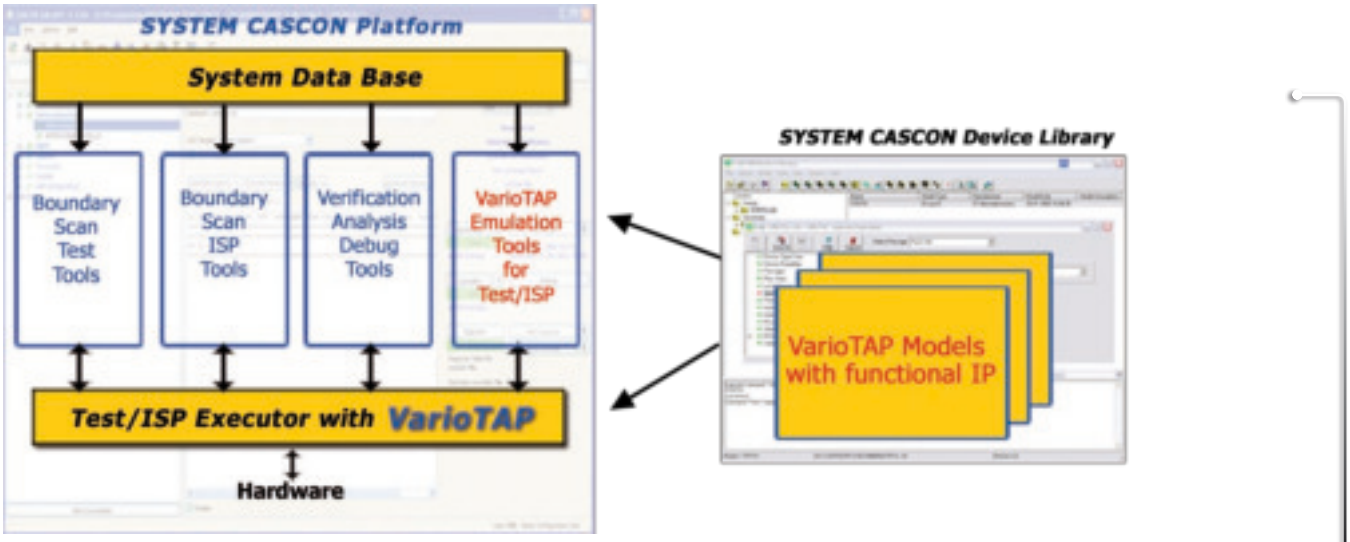
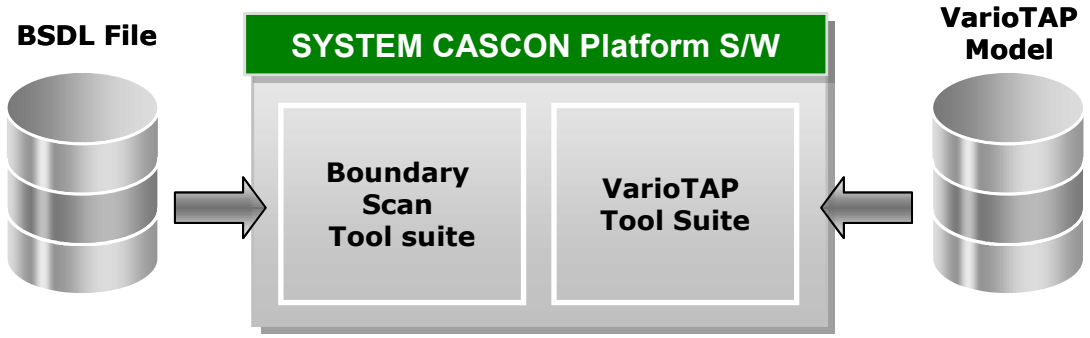


Figure 7 - Support of Boundary Scan, In-System programming and Emulation Test and in a single Integrated Development Environment (IDE)



- Specification of registers
- Type and mapping of BScan cells
- Definition of Op-codes
- Pin definitions

- Specification of emulations registers
- Behaviour model of the µP
- Definition of IP functions
- Pin reference

Figure 8 - Functional and structural description of the µP behaviour in VarioTAP® models, complementary to BSDL files for Boundary Scan

Summary

Boundary Scan and JTAG Emulation are two perfectly complementary methods, which are fused into one extremely flexible and powerful technique for advanced structural tests by GOEPEL electronic's VarioTAP® technology. The coherent implementation of this technology in the company's SYSTEM CASCON™ environment makes a smooth integration of JTAG Emulation tests into existing Boundary Scan projects possible. By combining the benefits of both methods, VarioTAP® provides a significantly higher test quality, shorter test and programming times, and higher quality of diagnostics with considerably reduced costs. The modular software IP based architecture, makes VarioTAP® completely independent of the target processor(s) and prepared for future applications and standards.

VarioTAP® logo

About GOEPEL electronic

GOEPEL electronic is a worldwide leading vendor of professional JTAG / Boundary Scan solutions and a technology innovator of IP based instrumentation. With more than 400 different products, GOEPEL electronic offers the currently most comprehensive and powerful portfolio in the market for Boundary Scan test, Flash programming, PLD programming, and JTAG emulation. A worldwide service network ensures the support for the globally more than 6,000 system installations. Founded 1991 and headquartered in Jena, Germany, GOEPEL electronic has currently about 160 employees and generated a revenue of 19.7 Million Euro in 2008. Further information about the company and its products and services can be found on the internet at **www.goepel.com**.

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[3] Jan Heiber - Boundary Scan versus Emulation Test, Proceedings of the NTF Forum 2008, Tallin

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Abbreviations and Acronyms

ATPG	Automated Test Program Generator
AVTG	Automated VarioTAP® Test Program Generator
BET	Bus Emulation Test
BScan	Boundary Scan
BSDL	Boundary Scan Description Language
BST	Boundary Scan Test
DFT	Design for Test (also DfT)
DUT	Device Under Test
FCT	Functional Circuit Test
FPT	Flying Probe Test
IC	Integrated Circuit (also referred to as "chip")
ICE	In-Circuit Emulation
ICP	In-Circuit Programming
ICT	In-Circuit Test
IEEE	Institute of Electrical and Electronics Engineers
IP	Intellectual Property
ISP	In-System Programming
JTAG	Joint Test Action Group
µC	Micro Controller
MCU	Micro Controller Unit
MDA	Manufacturing Defect Analyser
µP	Micro Processor
NPI	New Product Introduction
OCE	On-Chip Emulation
PCA	Printed Circuit Assembly
PLD	Programmable Logic Device
RAM	Random Access Memory
SET	System Emulation Test
SOC	System On Chip (also SoC)
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data In
TDO	Test Data Out
TMS	Test Mode Select
/TRST	Test Reset
UUT	Unit Under Test

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